The primary reference used in this rejection of claims will hereafter be referred to as the "Sturges Reference."

The Examiner has misperceived the teachings of the Sturges Reference; although this reference does indeed relate to cache management techniques, it fails to show numerous significant limitations of the present claims. More particularly, neither the Sturges Reference nor any other cited reference (as indicated in the last response filed by Applicant) shows Applicant's technique of implementing a spread memory layout, with page data effectively spread so as to not overwrite processing parameters that are to survive a cache reload. Importantly, the Sturges Reference does relate to a cache management technique, but it teaches that one should use a partition buffer (partition selector and mask) and partitioning of cache to resize cache to correspond to memory, not vice-versa; its teachings are very different than the present invention.

Applicant therefore respectfully requests reconsideration of the rejection of claims, and submits that all of the present claims are in condition for allowance.

I. The Sturges Reference.

The Sturges Reference is addressed to the problem of cache line replacement, and more particularly, to preventing items from being deleted which were expected to stay in cache for later use (paragraph 4). To solve this problem, the Sturges reference proposes a flexible system (paragraph 21) that addresses a number of specific embodiments, including the ability to provide inter-thread partitioning (paragraph 22), partitioning so as to segregate critical, real time data, from other data (paragraph 23), partitioning so as to segregate instructions and data (paragraph 24), and other embodiments. The goal of flexibility is achieved by dividing cache into a number of cache partitions, and using a refill mechanism that selects specific partitions in dependence upon a cache partition access table. "It is thus quite possible for an item to have access to more than one partition of cache, or indeed for an item to not be allowed access to the cache at all" (paragraph 10); "one or more cache partitions may be allocated to a page in main memory" (paragraph 15); the number and size of these partitions is dynamically alterable to provide the greatest flexibility possible (see, e.g., paragraph 20). The scheme of the Sturges Reference is succinctly illustrated by the cover figure of the Sturges Reference, FIG. 8.

II. Errors In The Present Rejection Of Claims.

It is the Examiner's position that the Sturges Reference shows a spread memory layout (false), with subsets of data mapped to a predetermined subset of each page (false), where each page is sized to map to quick access memory of a processor (false) - the Sturges Reference shows none of these things at all. Rather, as explained above, the Sturges Reference teaches that one should establish a buffer mechanism and programmable cache mask to provide the greatest flexibility possible - the Sturges Reference doesn't suggest specially configuring memory in advance for processing in cache, but rather, teaches specially configuring cache to be able to respond to a wide variety of different applications (for variable size, or any size pages). Indeed, as explicitly stated in the Sturges Reference, items can be stored in any number of partitions depending upon the memory and the application - see, e.g., paragraphs 10, 13, 15, 17, 46, 47, 48, 56 and 57 of the Sturges Reference; as succinctly stated in paragraph 48 of the Sturges Reference, "It is quite possible to allocate more than one bank to a page... in that case, if the line-in-page address has more bits than the row address for the cache, the partitions would behave as a k-way set associative cache where k partitions are allocated to a page... thus, in the described example the real page number of FIG. 3 can use banks B2 and B4... However, it may not use banks B1 and B3."

The Examiner in part has recognized some of the deficiencies of the Sturges Reference's teachings, stating "Sturges does not disclose the portions being less than the capacity of each page... At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the portions being less than the capacity of each page... One of ordinary skill in the art would have been motivated to do this in order to separate data from other information, thereby avoiding the risk of overwriting important information" (paragraph 3, pages 2-3, of the Office Action).

This position of the Examiner is improper; the Sturges Reference teaches a very specific cache mechanism, and teaches that the way to manage cache to avoid overwriting important information is by necessarily using a cache partition table and programmable mask - the Examiner's position that one should "disregard" these express teachings and instead

"magically" adopt Applicant's invention, and that somehow they would be motivated to do this even though the Sturges Reference teaches that it's necessary to use its solution, simply defies any justification in fact or law.

Applicant respectfully submits that the Examiner has misconstrued the Sturges Reference - It relates to specific cache structure, and differs fundamentally from Applicant's invention, which addresses memory organization to make, e.g., volume processing, more efficient in cache. The Sturges Reference is directed to a flexible cache structure that can be used in many applications, whereas the present invention is directed to a consistent memory organization that facilitates processing by cache and minimizes cache misses. There are substantial differences between the Sturges Reference and the present invention, and the Sturges Reference does not show most of the limitations of Applicant's claims.

III. The Present Rejection Under §103(a) Must Be Withdrawn.

35 U.S.C. §103(a) provides for unpatentability "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

A rejection for obviousness is based on the underlying factual inquiries set forth in *Graham v. John Deere:* (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the art; and (4) objective evidence of secondary considerations. *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, 796 F.2d 443, 447 (Fed. Cir. 1986).* Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. *In re Fritch, 972 F.2d 1260, 1266 (Fed. Cir. 1992).* The appropriate inquiry is *not* whether it would have been obvious to substitute an element, or modify the prior art, in a manner advanced by the Examiner, because that is not the appropriate test of patentability. *See, e.g., In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).* Rather, to meet its burden of showing prima facie obviousness, the PTO must necessarily show some objective teaching that would

lead one of ordinary skill to combine the relevant teachings to solve the problem confronting the applicant. *In re Fine, supra.*

1. **The Sturges Reference Has Been Misconstrued And Does Not Support The Rejection Of Any Of Applicant's Claims.**

In the present case, the differences between the present invention and the Sturges Reference are substantial. The Sturges Reference teaches that one must adopt a flexible solution adapted for different applications, and capable of accommodating variable page sizes, i.e., ones that may occupy one or several partitions in cache; viewed somewhat more abstractly, the Sturges Reference is directed to modifications of cache architecture to enable cache to be more flexibly operated. By contrast, the present invention is addressed to specially managing main memory, so that in active cache processing, memory calls and cache replacements inherently result in key parameters not being overwritten - Applicant's claim 1 is very specific in this regard, i.e., it recites "an apparatus comprising a data set stored on machine readable media", where the spread memory is implemented with multiple pages, each page having gaps (thereby creating a "spread") with the data portion being a subset of cache size and paginated and addressed such that as pages are loaded, data inherently goes into the same parts of cache, and the "gaps" leave other parts of cache unaffected.

The Sturges Reference takes a wholly different approach from the present invention and, other than suggesting the desirability of cache management and stating that pagination of memory is common, really shows none of the features of the present invention. For example, the Sturges Reference (comparing it to claim 1) does NOT show a spread memory layout, with data limited to a subset of each page, and page sizing deliberately made to conform to cache. The Sturges Reference does NOT show (comparing it to many of Applicant's dependent claims, e.g., claim 2) the formatting of memory to have identically sized data blocks; in fact, the Sturges Reference is very explicit about handling of variable size data blocks that can occupy multiple partitions. The Sturges Reference does NOT show dimensional interleaving or volumetric data processing (e.g., claims 2-3 and 12-14), where adjacent voxels are stored together in a contiguous data block in memory for more efficient graphics processing.

In short, Applicant respectfully submits that the rejection of claims over the Sturges Reference is erroneous, because one skilled in the art would not have considered Applicant's invention as obvious over the Sturges Reference in view of these differences; all evidence of record indicates that one examining the Sturges Reference would be lead to do *exactly* what the Sturges Reference *states should be done*, i.e., use a partition mask and partitioning of cache to flexibly manage cache, nothing more - there is no suggestion anywhere in the Examiner's relied upon references that indicates that one should ignore cache structure required by the Sturges Reference and instead manage memory and volumetric data sets per Applicant's teachings. If anything, the Sturges Reference would lead one skilled in the art away from Applicant's invention, not toward it.

2. **The Lauer Et Al. Patent Does Not Overcome Deficiencies In The Teachings Of The Sturges Reference; There is No Suggestion Or Teaching To Combine References.**

Applicant also contests the combination of the Lauer et al. Patent (US Patent 6,243,098) with the Sturges Reference, and associated obviousness rejection of claims 2, 3, 7-10, 12-14, 16, 17, 19, 20, 24-28, 30-32 and 35. As pointed out above, this rejection cannot stand because of the Examiner's improper reading on the Sturges Reference (which is used as the primary reference). However, Applicant also wishes to contest the act of aggregating the Lauer et al. Patent with the Sturges Reference; there clearly is no teaching or suggestion to make this combination.

As pointed out in Applicant's prior response, the primary problem faced by Applicant is delays caused by cache misses for needed processing parameters (as opposed to voxel data); to address this problem, Applicant's invention calls for a spread memory layout, with pages of specific size and format that effectively force group loading of image data always into a predetermined subset of cache, so as to deliberately put image data in a cache in a manner that will not cause unintended cache discard of processing parameters.

Viewed against this problem, the Lauer et al. Patent is directed to enabling real time raycasting on laptops and workstations, and it teaches that in order to solve this problem, one must use parallel processing and four specific processing techniques, including "blocking", "sectioning," "pin-reduction" and "mini-blocking". The approach of the Lauer et al. Patent is that these things are processing shortcuts that speed up processing; the Lauer et al. Patent does not address memory organization apart from stating that adjacent data should be stored in an adjacent manner (the so-called "blocking" technique of the Lauer et al. Patent.). As has been acknowledged by the Examiner, the Lauer et al. Patent does not show a spread memory layout and it also doesn't provide any teaching or suggestion as to how one can avoid or minimize cache discard of image processing parameters.

The Sturges Reference provides no hint, suggestion, inference, or other admonition that one should use oct-tree addressing or dimensional interleaving as specified by Applicant's disclosure - there is nothing at all of evidence in this case that would indicate that one skilled in the art would have been lead to specifically to combine the Sturges Reference and the Lauer et al. Patent in order to make structure combinations deemed useful by the Examiner in rejecting Applicant's claims.

As indicated already, the appropriate legal inquiry is *not* whether it would have been obvious to substitute an element, or modify the prior art, in a manner advanced by the Examiner, because that is not the appropriate test of patentability. *See, e.g., In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).* Rather, to meet its burden of showing prima facie obviousness, the PTO must necessarily show some objective teaching that would lead one of ordinary skill to combine the relevant teachings to solve the problem confronting the applicant. *In re Fine, supra.*

Clearly, the Examiner has not met this burden in this case; even if the Examiner could meet this burden, the Lauer et al. Patent does not supply any of the missing teachings or differences between Applicant's base claims and the Sturges Reference; other than the "blocking" technique of the Lauer et al. Patent, neither reference deals with memory management. For these reasons, Applicant respectfully requests that the rejection of claims 2-3, 7-10, 12-14, 16-17, 19-20, 20, 24-28, 20-32 and 35 be withdrawn.

In summary, Applicant submits that the present rejection of claims over the Sturges Reference alone or in combination with the Lauer et al. Patent is erroneous; Applicant respectfully requests that the allowance of claims 18-28 be restored, and submits that all of claims 1-36 are allowable over the cited art. Accordingly, Applicant respectfully prays for a notice of allowance.

Respectfully Submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being sent via facsimile transmission to the United States Patent and Trademark Office, at telephone/facsimile number (703) 872-9306 on this 31 August 2004.

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Dated: 31 August 2004